CLAIMS

What is Claimed is:

1. A GaN substrate including a GaN (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, at an offcut angle in a range that is from about 0.2 to about 10 degrees, wherein said surface has a RMS roughness measured by 50 x 50μm^2 AFM scan that is less than 1 nm, and a dislocation density that is less than 3E6 cm^{-2}.

2. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut predominantly toward the $<10\bar{1}0>$ direction.

3. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut predominantly toward the $<11\bar{2}0>$ direction.

4. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut at an offcut angle in a range of from about 0.2 to about 4 degrees.

5. The GaN substrate of claim 4, wherein the GaN (0001) surface is offcut toward the $<10\bar{1}0>$ direction.

6. The GaN substrate of claim 4, wherein the GaN (0001) surface is offcut toward the $<11\bar{2}0>$ direction.

7. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut at an offcut angle in a range of from about 3 to about 8 degrees.

8. The GaN substrate of claim 7, wherein the GaN (0001) surface is offcut toward the $<10\bar{1}0>$ direction.

9. The GaN substrate of claim 7, wherein the GaN (0001) surface is offcut toward the $<11\bar{2}0>$ direction.

10. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut at an offcut angle in a range of from about 2.5 to about 8 degrees.

11. The GaN substrate of claim 10, wherein the GaN (0001) surface is offcut toward the $<10\bar{1}0>$ direction.

12. The GaN substrate of claim 10, wherein the GaN (0001) surface is offcut toward the $<11\bar{2}0>$ direction.

13. The GaN substrate of claim 1, wherein said surface has a RMS roughness measured by 50 x 50μm^2 AFM scan that is less than 0.9 nm.

14. The GaN substrate of claim 1, wherein said surface has a RMS roughness measured by 50 x 50μm^2 AFM scan that is less than 0.5 nm.

15. The GaN substrate of claim 1, wherein said surface has a dislocation density that is less than 1E6 cm^{-2}.

16. The GaN substrate of claim 1, wherein said surface has a dislocation density that is less than 5E5 cm^{-2}.

17. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut at an offcut angle in a range of from about 2.5 to about 10 degrees.

18. The GaN substrate of claim 1, wherein the GaN (0001) surface is offcut at an offcut angle in a range of from about 5 to about 8 degrees.

19. A microelectronic or opto-electronic device article, comprising a GaN substrate as claimed in claim 1, and a microelectronic or opto-electronic device structure including a homoepitaxial GaN layer deposited on said surface.

20. The microelectronic or opto-electronic device article of claim 19, wherein said microelectronic or opto-electronic device structure comprises a device selected from the group consisting of laser diodes, light emitting devices, transistors, diodes, and detectors.

21. The device article of claim 19, wherein said device structure comprises a blue or shorter wavelength laser diode, or an HEMT device.

22. A method of forming a GaN substrate including a GaN (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, at an offcut angle in a range that is from about 0.2 to about 10 degrees, wherein said surface has a RMS roughness measured by 50 x 50μm^2 AFM scan that is less than 1 nm, and a dislocation density that is less than 3E6 cm^{-2}, said method including growing a bulk GaN single crystal body, and processing said bulk GaN single crystal body to form at least one wafer therefrom, wherein said processing step includes a step selected from the group consisting of: (i) a slicing step conducted in a slicing plane tilted away from the c-plane at said offcut angle in said direction selected from the group consisting of $<10\bar{1}0>$ and

<11$\bar{2}$0> directions, (ii) an angle lapping step conducted in a lapping plane tilted away from the c-plane at said offcut angle in said direction selected from the group consisting of <10$\bar{1}$0> and <11$\bar{2}$0> directions, and (iii) separating said bulk GaN single crystal body after growing said bulk GaN single crystal body on a vicinal heteroepitaxial substrate including a (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of <10$\bar{1}$0> and <11$\bar{2}$0> directions, at an offcut angle in said range of from about 0.2 to about 10 degrees.

23. The method of claim 21, wherein said at least one wafer is finished by at least one finishing step selected from the group consisting of lapping, polishing and chemical mechanical polishing.

24. The method of claim 21, wherein said processing step includes step (i).

25. The method of claim 21, wherein said processing step includes step (ii).

26. The method of claim 21, wherein said processing step includes step (iii).

27. The method of claim 25, wherein said vicinal heteroepitaxial substrate comprises a material selected from the group consisting of sapphire and GaAs.

28. A method of fabricating a microelectronic or opto-electronic device, comprising

(c) forming a GaN substrate including a GaN (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of <10$\bar{1}$0> and <11$\bar{2}$0> directions, at an offcut angle in a range that is in a range of from about 0.2 to about 10 degrees, wherein said surface has a RMS roughness measured by

50 x 50μm AFM scan that is less than 1 nm, and a dislocation density that is less than 3E6 cm^{-2}, said method including growing a bulk GaN single crystal body, and processing said bulk GaN single crystal body to form at least one wafer therefrom, wherein said processing step includes a step selected from the group consisting of: (i) a slicing step conducted in a slicing plane tilted away from the c-plane at said offcut angle in said direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, (ii) an angle lapping step conducted in a lapping plane tilted away from the c-plane at said offcut angle in said direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, and (iii) separating said bulk GaN single crystal body after growing said bulk GaN single crystal body on a vicinal heteroepitaxial substrate including a (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, at an offcut angle in said range of from about 0.2 to about 10 degrees, and

(d) depositing on said GaN substrate a homoepitaxial III-V nitride material.

29. The method of claim 27, wherein said step of depositing a homoepitaxial III-V nitride material comprises MOVPE.

30. The method of claim 27, wherein said depositing step is carried out at a temperature in a range of from about 1100 to about 1225°C.

31. The method of claim 27, wherein said depositing step is carried out at temperature in a range of from about 1100 to about 1225°C.

32. The method of claim 27, wherein said depositing step is carried out at temperature in a range of from about 1120 to about 1170°C.

33. The method of claim 27, wherein said depositing step is carried out at temperature in a range of from about 700 to about 1220°C.

34. The method of claim 27, wherein said depositing step is carried out at growth rate in a range of from about 0.1 μm/hr to about 50 μm/hr.

35. The method of claim 27, wherein said depositing step is carried out at growth rate in a range of from about 1 μm/hr to about 4 μm/hr.

36. The method of claim 27, wherein said depositing step is carried out at growth rate in a range of from about 2 μm/hr to about 4 μm/hr.

37. The method of claim 27, wherein said homoepitaxial III-V nitride material comprises GaN.

38. The method of claim 35, further comprising depositing an AlGaN material on the GaN, to form an AlGaN/GaN HEMT.

39. A III-V nitride substrate including a (Al,In,Ga)N (0001) surface offcut from the <0001> direction predominantly towards a direction selected from the group consisting of $<10\bar{1}0>$ and $<11\bar{2}0>$ directions, at an offcut angle in a range that is from about 0.2 to about 10 degrees, wherein said surface has a RMS roughness measured by 50 x 50μm^2 AFM scan that is less than 1 nm, and a dislocation density that is less than 3E6 cm^{-2}.